Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 11. (canceled)

12. (Currently amended) ~~A~~ The data transmitter according to claim 35, wherein the signal transmitter comprises~~configured and arranged to receive a plurality of input signals and to transmit a plurality of first output signals and a plurality of second output signals, each of the first and second output signals corresponding to a different one of the input signals and each being transmitted along a corresponding one of a plurality of conductive paths, said data transmitter comprising~~:

a plurality of first latches, each having (1) a clock input configured and arranged to receive a first clock signal including a series of first transitions, with consecutive first transitions being separated by ~~a~~ the ~~time~~ clock period T_CLK, (2) a latch input configured and arranged to receive a corresponding one of the input signals, and (3) an latch output configured and arranged to produce a corresponding latch signal, each first latch being further configured and arranged to latch a data value from the corresponding input signal to the corresponding latch signal upon each first transition; and

a plurality of second latches, each having (1) a clock input configured and arranged to receive a second clock signal based on the first clock signal and including a series of second transitions, with consecutive second transitions being separated by ~~a~~ the ~~time~~ clock period T_CLK, (2) a latch input configured and arranged to receive a corresponding input signal, and (3) a latch output configured and arranged to produce a corresponding latch signal, each second latch being further configured and arranged to latch a data value from the corresponding input signal to the corresponding latch signal upon each second transition;

wherein each first output signal is based on a latch signal of a different one of the first latches and each second output signal is based on a latch signal of a different one of the second latches, and

wherein a time between a transition on an input signal and a corresponding transition on a corresponding second output signal exceeds a time between a transition on an input signal and a corresponding transition on a corresponding first output signal by a delay period T_DLY, and

wherein the time period T_CLK is greater than the delay period T_DLY, and

wherein adjacent conductive paths that each carry one of the plurality of first output signals are separated by a conductive path that carries one of the plurality of second output signals.

13. (Original) The data transmitter according to claim 12, wherein the data transmitter and the plurality of conductive paths are fabricated on the same semiconductor substrate.

14. (Original) The data transmitter according to claim 12, wherein the data transmitter is further configured and arranged to receive an operating voltage from two power rails, and

wherein the two power rails are parallel to and on opposite sides of the plurality of conductive paths.

15. (Original) The data transmitter according to claim 12, wherein each one among the plurality of conductive paths includes a corresponding one of a plurality of parallel transmission lines, and

wherein the data transmitter is further configured and arranged to couple the first clock signal to one of the plurality of parallel transmission lines.

16. (Original) The data transmitter according to claim 12, said data transmitter further comprising a plurality of buffers, each buffer being coupled to a different one of the latch outputs of the first and second latches.

17. (Original) The data transmitter according to claim 12, said data transmitter further comprising a delay element configured and arranged to receive the first clock signal and to produce the second clock signal,

wherein the second clock signal is delayed with respect to the first clock signal by the delay period T_DLY.

18. (Original) The data transmitter according to claim 12, said data transmitter further comprising a plurality of delay elements, each configured and arranged to receive a different one of the second latch signals and to produce the corresponding second output signal.

19. (Original) The data transmitter according to claim 18, wherein the second clock signal is substantially identical to the first clock signal.

20. (Original) The data transmitter according to claim 12, wherein the delay period T_DLY is at least twice as long as a rise time of the data clock signal.

21. – 34. (canceled)

35. (New) A data transmitter configured and arranged to receive a plurality of input signals and to transmit a plurality of first output signals and a plurality of second output signals, each of the first and second output signals corresponding to a different one of the input signals and each being transmitted along a corresponding one of a plurality of conductive paths, said data transmitter comprising:

a signal transmitter for sending each one of the plurality of first and second output signals on a respective one of substantially parallel conductors of a bus, with transmissions on each one of the substantially parallel conductor separated by a time period substantially equal to a clock period T_CLK; and

a delay generator for delaying said second output signals by a delay period T_DLY relative to said first output signals so that a first time between a transition on an input signal and a corresponding transition on a corresponding second output signal exceeds a second time between a transition on an input signal and a corresponding transition on a corresponding first output signal by the delay period T_DLY,

wherein the clock period T_CLK is greater than the delay period T_DLY, and wherein adjacent conductive paths that each carry one of the plurality of first output signals are separated by a conductive path that carries one of the plurality of second output signals.

36. (New) The data transmitter according to claim 35, further configured and arranged to transmit a plurality of third output signals, each of the first, second and third output signals corresponding to a different one of the input signals and each being transmitted along a corresponding one of the plurality of conductive paths, wherein said signal transmitter is adapted for sending each of said third output signals on a respective one of the substantially parallel conductors of a bus with transmissions separated by the time period substantially equal to the clock period T_CLK, and the delay generator is adapted for delaying said third output signals by a delay time relative to said second output signals so that a third time between a transition on an input signal and a corresponding transition on a corresponding third output signal exceeds the second time between the transition on the input signal and the corresponding transition on the corresponding second output signal by the delay time greater than the delay period T_DLY but less than the clock period T_CLK, and wherein the adjacent conductive paths that each carry one of the plurality of first output signals are separated

by the conductive path that carries one of the plurality of second output signals and by a conductive path that carries one of the plurality of third output signals.